Power MOSFET

30 V, 59 A, Single N-Channel, SO-8 FL

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Low RG
- These are Pb-Free Device*

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

			Sym-		
Parameter			bol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current R _{θJA} (Note 1)		T _A = 25°C T _A = 85°C	I _D	13.5 9.7	Α
Power Dissipation R _{θJA} (Note 1)		T _A = 25°C T _A = 85°C	P _D	2.16 1.1	W
Continuous Drain Current R _{θJA} ≤10 s	Steady State	T _A = 25°C T _A = 85°C	I _D	21.8 15.7	Α
Power Dissipation $R_{\theta JA} \leq 10 \text{ s}$		T _A = 25°C T _A = 85°C	P _D	5.7 2.9	W
Continuous Drain Current R _{θJA} (Note 2)		T _A = 25°C T _A = 85°C	I _D	8.6 6.2	Α
Power Dissipation R _{θJA} (Note 2)		T _A = 25°C T _A = 85°C	P _D	0.87 0.45	W
Continuous Drain Current R _{θJC} (Note 1)		T _C = 25°C T _C = 85°C	I _D	59 42.5	Α
Power Dissipation $R_{\theta JC}$ (Note 1)		T _C = 25°C T _C = 85°C	P _D	41.7 21.7	W
Pulsed Drain Current	t _p = 10 μs	T _A = 25°C	I _{DM}	177	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to +150	°C
Source Current (Body Diode)			I _S	35	Α
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 24 V, V _{GS} = 10 V, I _L = 25.6 A, L = 0.3 mH, R _G = 25 Ω)			EAS	98	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

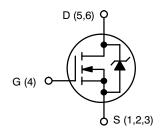
- 1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.



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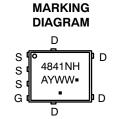
http://onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
30 V	7.0 mΩ @ 10 V	50 A
30 V	11.6 mΩ @ 4.5 V	59 A



N-CHANNEL MOSFET





= Assembly Location

= Year

= Work Week WW

= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFS4841NHT1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NTMFS4841NHT3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{ heta JC}$	3	
Junction-to-Ambient - Steady State (Note 1)	$R_{ heta JA}$	57.8	2004
Junction-to-Ambient - Steady State (Note 2)	$R_{ heta JA}$	143.5	°C/W
Junction-to-Ambient (t≤10 s)	$R_{\theta JA}$	22.1	

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS						•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				28		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25 °C T _J = 125 °C			1	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 250 μA	1.5	2.1	2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V to	I _D = 30 A		4.8	7.0	
		11.5 V	I _D = 15 A		4.8		mΩ
		V _{GS} = 4.5 V	I _D = 30 A		8.8	11.6	
			I _D = 15 A		8.5		
Forward Transconductance	9FS	V _{DS} = 1.5 V, I _D = 50 A			57		S
CHARGES AND CAPACITANCES				•	•	•	•
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 12 V			1565	2113	pF
Output Capacitance	C _{OSS}				325	439	
Reverse Transfer Capacitance	C _{RSS}				173	268	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A			11.3	16.7	nC
Threshold Gate Charge	Q _{G(TH)}				1.4	2.1	
Gate-to-Source Charge	Q_{GS}				5.3	7.9	
Gate-to-Drain Charge	Q_{GD}				4.5	6.8	1
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 11.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_{D} = 30 \text{ A}$			24.4	33	nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn-On Delay Time	t _{d(ON)}				12.1	18.1	
Rise Time	t _r	V_{GS} = 4.5 V, V_{DS} = 15 V, I_{D} = 15 A, R_{G} = 3.0 Ω			23.3	34.9	ns
Turn-Off Delay Time	t _{d(OFF)}				14.1	21.1	
Fall Time	t _f				4.9	7.3	
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 11.5 V, V_{DS} = 15 V, I_{D} = 15 A, R_{G} = 3.0 Ω			7.2	10.7	
Rise Time	t _r				20.6	30.9	7
Turn-Off Delay Time	t _{d(OFF)}				21.9	32.9	ns
Fall Time	t _f				2.9	4.4]

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
DRAIN-SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.86	1.2		
		$V_{GS} = 0 \text{ V},$ $I_{S} = 30 \text{ A}$	T _J = 125°C		0.71		V	
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_S/dt = 100 \text{ A/}\mu\text{s,}$ $I_S = 30 \text{ A}$			18.8		ns	
Charge Time	t _a				11.4			
Discharge Time	t _b				7.4			
Reverse Recovery Charge	Q _{RR}				6.7		nC	
PACKAGE PARASITIC VALUES								
Source Inductance	L _S	- - T _A = 25°C			0.93		nH	
Drain Inductance	L _D				0.005		1	
Gate Inductance	L _G				1.84		1	
Gate Resistance	R _G	1			0.90		Ω	

^{3.} Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%. 4. Switching characteristics are independent of operating junction temperatures.

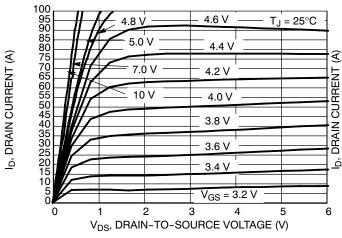


Figure 1. On-Region Characteristics

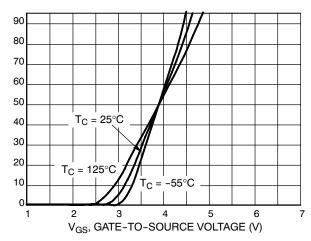


Figure 2. Transfer Characteristics

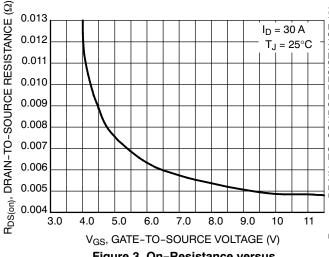


Figure 3. On-Resistance versus Gate-to-Source Voltage

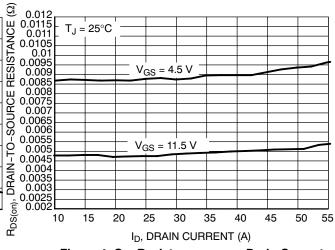


Figure 4. On-Resistance versus Drain Current and Gate Voltage

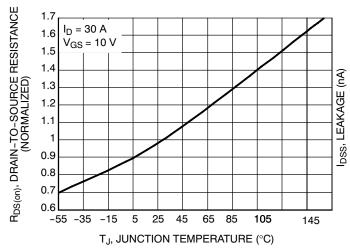


Figure 5. On–Resistance Variation with Temperature

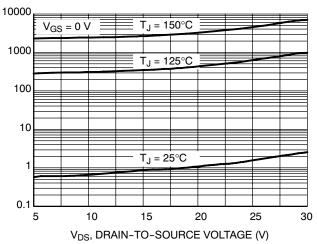


Figure 6. Drain-to-Source Leakage Current versus Voltage

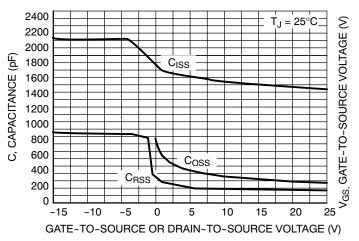


Figure 7. Capacitance Variation

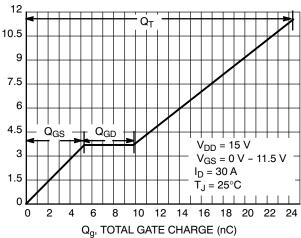


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

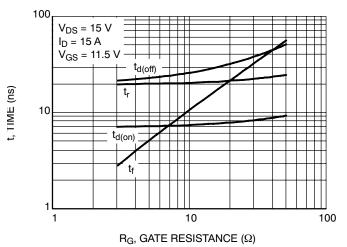


Figure 9. Resistive Switching Time Variation versus Gate Resistance

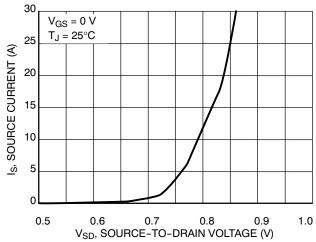


Figure 10. Diode Forward Voltage versus
Current

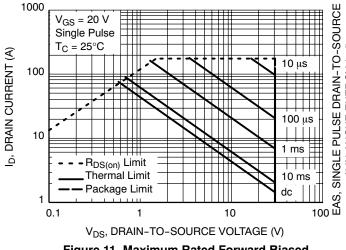


Figure 11. Maximum Rated Forward Biased Safe Operating Area

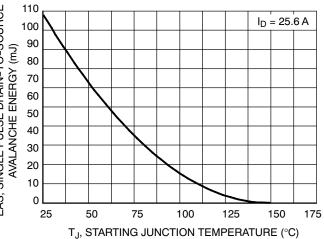


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

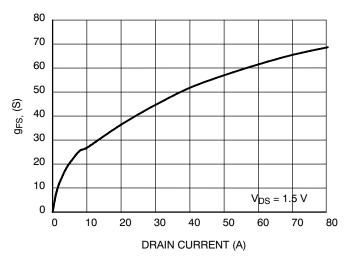
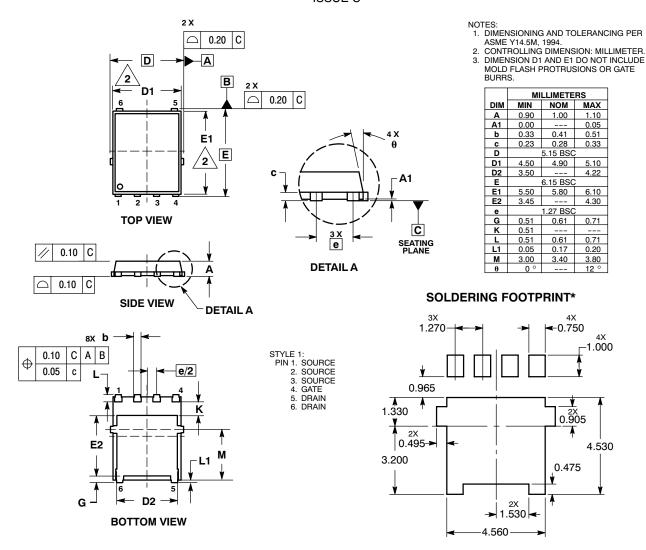


Figure 13. G_{FS} versus Drain Current

PACKAGE DIMENSIONS

DFN6 5x6, 1.27P (SO8 FL) CASE 488AA-01 ISSUE C



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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